FPGA-based Image Acquisition Integrated Circuit Design

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Abstract: In the information era, image acquisition and processing technology are becoming more widespread. With the birth of big data, the amount of image information on the Internet has become geometrically graded. Therefore the traditional image acquisition and processing system no longer apply to the present image acquisition preprocessing process. This text, in this background, designed a kind of FPGA-based image acquisition integrated circuit, using a large-scale integrated circuit to carry out image acquisition processing. First, this paper carried out hardware and basic principle analysis of the FPGA chip, and based on this, the VGA display part of the digital integrated circuit was redesigned and then ensured that its power consumption was within the normal level, then the use of the edge image detection algorithm further optimized the FPGA's work efficiency and significantly improved chip efficacy.

1. Introduction

1.1 FPGA Overview and Basic Structure Principle

The FPGA circuit is mainly used for image preprocessing, including image noise removal, image filtering, image compression and restoration, and edge segmentation. FPGA is mainly a collection of programmable logic elements composed of large-scale integrated circuits. The FPGA image preprocessing interface circuit board component is one of the core parts of the FPGA image preprocessing component, and its assembly quality will directly affect the performance and service life of the overall FPGA image preprocessing product. Therefore, the FPGA image preprocessing assembly process is highly valued and widely concerned. At present, the assembly of FPGA image preprocessing interface circuit board components is usually completed on a semi-automated assembly line, which has low assembly quality and poor assembly reliability. It mainly relies on manual design and coding for assembly, and the manual design and coding method has the problems of high labor intensity and low labor efficiency, so it cannot meet the stability and reliability requirements of mass production [1].

1.2. FPGA Design Methodology

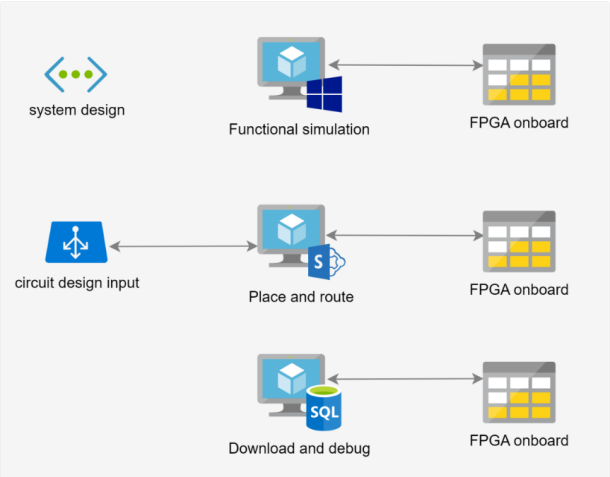

Figure 1 FPGA design flow

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Figure 1 illustrates the FPGA design process, which consists primarily of system design, circuit simulation input, functional simulation, comprehensive simulation, and layout and routing. Finally, the FPGA is programmed into the database on board. Image preprocessing design coding technology uses image sensors specified images for the target at the beginning of this research. The development of industrial automation and computer technology has led to the rapid development of the image preprocessing design coding method, which has become widely used in the semiconductor and electronic industries, mainly for assembly and surface mount technology, etc., as well as in the manufacturing and processing of electronic products. In this century, as the informatization process has developed, this technology has also attempted to connect with the Internet of Things.

FPGA image preprocessing system is mainly divided into embedded FPGA image preprocessing systems and large-scale integrated FPGA image preprocessing systems.

(1) Embedded FPGA image preprocessing system: usually referred to as a smart camera, it works through a highly integrated FPGA image preprocessing system. This system integrates information processing and recognition, image acquisition and recording, and communication connection functions and can complete sampling alone, analysis, upload, and other functions independently. With modular features and high reliability, each part of the functional module can be replaced separately.

(2) FPGA image preprocessing system based on large-scale integration: This type of system achieves detection requirements through high configuration, and a single-chip computer or microcomputer usually realizes its chip circuit board, and due to its large-scale integration characteristics, it has good scalability and flexible design. It has a high degree and can be used to upgrade the customer's later requirements. However, this type of system is generally large in size and requires a large installation space, so the system stability is not high and is insufficiently applied in the actual industrial environment [2].

1.3 FPGA Software and Hardware Development Platform and Coding Method

The total image processing power consumption of the digital FPGA image preprocessing circuit is shown in the following formula: the static image processing power consumption, the last two items are the switching image processing power consumption and the short-circuit image processing power consumption, respectively. Where I_{leakage} is the leakage current, V_{dd} is the power supply voltage for the gate FPGA image preprocessing circuit, α is the flip frequency of the gate FPGA image preprocessing circuit network, f is the clock frequency, C is the total load capacitance of the FPGA image preprocessing circuit, I_{st} is a switch short-circuit FPGA image preprocessing circuit. From the image processing power consumption formula, it can be seen that the design can be comprehensively considered from these parameters [3].

$$P = \sum I_{\text{kakage}} V_{di} + \sum \frac{1}{2} \alpha f C V_{dd}^2 + \sum I_{st} V_{dl} \tag{1}$$

In this process, the low-power limited encoding process of state transition is shown in the following formula, where formula represents the state transition of input and output, which is used for low-power FPGA circuit board coding arrangement.

$$P_{ij} = P\left(s = s_j \mid s = s_i\right) = \frac{N_{ij}}{N} \tag{2}$$

Where, P_{ij} is the FPGA coding arrangement s_i jump s_j to jump probability, N_{ij} arrange the number of s_i jumps s_j for the FPGA code, N arranges the number of jumps for all FPGA codes [4].

2. FPGA Image Acquisition Integrated Circuit Design

2.1 Overall Design of Image Acquisition Integrated Circuit System

Under the above coding arrangement feature value, the state machine of FPGA encodes binary features as shown in the following formula.

$$X = \begin{pmatrix} x1 \\ x2 \\ x3 \\ x4 \\ x5 \end{pmatrix} = \begin{pmatrix} x11 & x12 & x13 & x14 & x15 \\ x21 & x22 & x23 & x24 & x25 \\ x31 & x32 & x33 & x34 & x35 \\ x41 & x42 & x43 & x44 & x45 \\ x51 & x52 & x53 & x54 & x55 \end{pmatrix} \tag{3}$$

In this process, the inversion function of the system encoding is as follows under the low-power encoding feature:

$$f = \sum_{i=1}^{n} \sum_{j=i+1}^{n} \left[\left(P_{ij} + P_{ji} \right) \times \sum_{k=1}^{s} \left(x_{ik} \oplus x_{jk} \right) \right] \tag{4}$$

The overall design requirements of the image acquisition integrated circuit system are divided into the following categories:

(1) FPGA image preprocessing accuracy: Constrained by the FPGA image preprocessing error rate, class A requires an error rate of 0.1%, and class B requires an error rate of 0.2%.

(2) FPGA image preprocessing speed: The measurement standard of FPGA image preprocessing speed is a complete process from forming into the pipeline to completing the FPGA image preprocessing and entering the information database. Among them, the FPGA image preprocessing time is less than 8s when the image preprocessing interface enters the camera's line of sight.

(3) Information warehousing and result storage: the result display is identified by qualified and unqualified; statistical data mainly records the number of qualified and unqualified workpieces; The system should work in both online and offline states, and there should be corresponding backups to save the image content; It should be able to switch between different identification data and identification programs for different types of picture preprocessing interface circuit boards.

2.2 Design of Image Acquisition and Processing Module

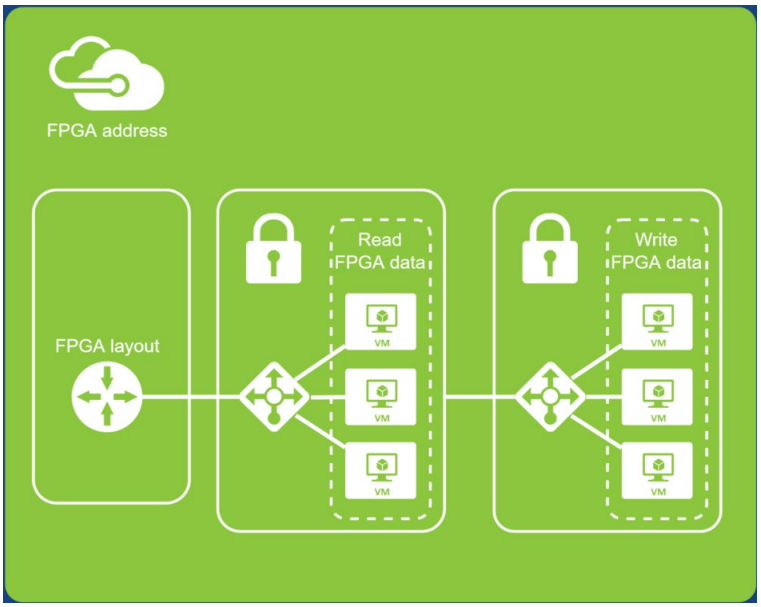

Figure 2 FPGA image acquisition and processing module design flow

The design flow of the FPGA image acquisition and processing module is shown in Figure 2.

When performing size inspection on FPGA large-scale integrated circuits, it should be judged according to the size, location, and quantity of components, and different types of component defects should be recorded. In general, there are the following five categories of defects:

(1) Missing components: Missing components on the FPGA large-scale integrated circuit are generally caused by component collisions on the assembly line.

(2) Missing component process: The large-scale integrated B-board printing process is missing.

(3) Mixed assembly of components: the position of the original image preprocessing is wrong or misplaced.

(4) The pins of the original piece of image preprocessing are broken: the pins of the original piece of component image preprocessing are missing.

(5) The Image preprocessing original sheet is not pressed and packaged in place: the image preprocessing original sheet is not completely installed in the FPGA large-scale integrated circuit [5].

2.3 Control and Display Module Design

There are defects in applying large-scale integrated FPGA image preprocessing systems in traditional industrial industries, such as poor system stability in the development cycle and later maintenance. Therefore, embedded systems are used for solution design. In this design, the installation space provided by the image preprocessing interface circuit board assembly line is limited, so the installation space of the large-scale integrated FPGA image preprocessing system is insufficient [6].

The selection criteria for the display module of the FPGA image preprocessing device are as follows:

(1) The image sensor chip needs to be matched.

(2) Determine whether the measured object requires the display module of the linear array FPGA image preprocessing device or the display module of the area array FPGA image preprocessing device.

(3) Determine whether the display module of the color FPGA image preprocessing device is required according to the color resolution requirements.

(4) Select the display module frequency of the FPGA image preprocessing device according to the speed requirement of dynamic detection.

(5) Determine the resolution of the display module of the FPGA image preprocessing device according to the system detection accuracy requirements.

The selection criteria for industrial FPGA image preprocessing display device are as follows:

(1) Working wavelength, frequency conversion, and fixed frequency: choose according to whether the working distance changes.

(2) Depth of field and FPGA image preprocessing display device type: select according to the position and wide angle of the image preprocessing part.

(3) The selection of image processing size and the determination of the field of view image processing angle: determined according to the scope of image processing required.

3. FPGA Image Acquisition Integrated Circuit Preprocessing Algorithm

3.1 Image Edge Detection Algorithm

Under the low-power encoding feature, the address encoding of the FPGA asynchronous depth image edge detection algorithm is as follows.

$$addr=\begin{cases}2^{n-1}-k & \text{k=1}\\ 2^{n-1}-k & addr=2^{n-1}+k-1\\ addr+1 & \text{k=0}\end{cases} \tag{5}$$

Where k is the system depth of the FPGA asynchronous depth image edge detection algorithm.

The image captured by the image preprocessing machine is generally two-dimensional, and the feature recognition of the workpiece contour needs to extract its three-dimensional feature

information. Therefore, the feature transformation of the position structure is firstly performed on the picture's coordinate system, which mainly relies on the translation and rotation of the coordinate system of the FPGA chip processing module, and the reference system transformation is performed on it. Image preprocessing edge algorithm, as a classic image processing algorithm in deep learning, has been widely used in the field of image processing and recognition. In this process, the image preprocessing edge algorithm requires less parameters than other image processing algorithms and can directly input the original image to perform corresponding processing operations, so it has been widely and profoundly used in this field [7].

The FPGA image preprocessing method refers to a system that recognizes, measures, judges, and classifies objects and human targets through FPGA image sensors. At the beginning of this research, the specified images were obtained for the target through corresponding technical means. With the high development of industrial automation and computer technology, the FPGA image preprocessing method has emerged as the times require and is widely used in the semiconductor and electronic industries, mainly for assembly and surface mount processes, etc., and also in the electronic product processing industry. With the gradual development of the informatization process in this century, this technology is also trying to connect with the Internet of Things. With the rapid development of the informatization process, the FPGA image preprocessing method and technology have begun appearing in large-scale industrial applications. At the beginning of this research, the specified images were obtained for the target through corresponding technical means. With the high development of industrial automation and computer technology, the FPGA image preprocessing method has emerged as the times require and is widely used in the semiconductor and electronics industry, mainly for assembly and surface mount processes, etc., and for the electronic product processing industry. FPGA image preprocessing method technology is mainly used in tobacco, textile, video packaging, agricultural product color sorting, and other industries on a large scale in my country. It is also used in the image edge preprocessing described in this paper.

3.2 Improved Adaptive Image Filtering Method

The traditional improved adaptive filtering algorithms have many defects, and their mean value of improved adaptive filtering accuracy is not very accurate. Therefore, this paper designs a collaborative neighbor algorithm based on the image adaptive fringe field improved adaptive filtering. The nearest neighbor collaborative algorithm is one of the most typical algorithms in the mean-improved adaptive filtering collaborative algorithm. This algorithm extracts the image adaptive edge features for the image adaptive edge based on the image adaptive edge preference. The feature of this algorithm is that it will improve adaptive filtering on the adaptive edge of the picture with similar characteristics of the improved adaptive filtering, divide it according to the group, and divide each other into neighbors. Then, according to the preference of the adaptive edge of the adjacent pictures, the average value of the group of the adaptive edge of other pictures in the group is improved to filter similar features adaptively.

This algorithm mainly relies on the image adaptive edge set to work, and for the division of the image adaptive edge set, it mainly uses the method of event space visualization to divide the image adaptive edge score matrix. During the division process, the internal elements in the matrix are inserted, such as the improved adaptive filtering feature of the picture adaptive edge, the picture adaptive edge level, the picture adaptive edge type, etc. In this way, the features of the adaptive edge of the picture can be accurately modeled [8].

3.3 Grayscale Circuit Design of FPGA Image Acquisition System

The design flow of the grayscale circuit of the FPGA image acquisition system is shown in Figure 3 below. The figure mainly shows the main circuit design process of the FPGA picture adaptive acquisition method [9]. First, after tape-out, a grayscale PCB board is initially made, and then the chip address is called by writing the address of the FPGA picture adaptive acquisition method. FPGA image self-adaptive acquisition method addresses call and read to complete the overall FPGA image acquisition system grayscale circuit production process.

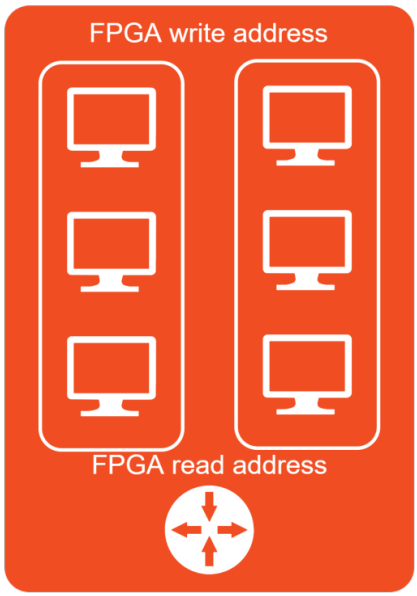

Figure 3 Design flow of grayscale circuit of FPGA image acquisition system

A major feature of the grayscale circuit of the FPGA image acquisition system is to convert the image received by the system into a grayscale image that the computer can recognize [10].

4. Conclusion

This paper introduces and analyzes the current image preprocessing algorithm, highlighting its shortcomings. In view of its slow efficiency, the large-scale integrated FPGA chip is used to update and improve the image preprocessing algorithm to make it suitable for the image preprocessing acquisition system. On this basis, this paper deeply designs the part of the FPGA chip used for image preprocessing and uses the image edge algorithm to improve the chip's efficiency significantly.

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